

Appl. No. 09/801,564
Amdt. dated June 14, 2005
Preliminary Amendment

PATENT

REMARKS/ARGUMENTS

Interview

On June 8, 2005, the Examiner granted an interview to discuss the current status of the rejections. Granting of interviews is always appreciated. No final agreement was reached, but this response is believed to address the Examiner's concerns expressed in the interview.

35 U.S.C. §103 Rejections

The final Office Action and the Advisory Action has rejected claims 1-2, 4-7, 9-13, 15-16 and 18-22 under 35 U.S.C. §103(a) as being obvious over the cited portions of U.S. Patent No. 5,959,874 to Lin et al. (hereinafter "Lin") in view of the cited portions of non-patent literature document "8XC251SB Embedded Microcontroller User's Manual" of Intel Inc. (hereinafter "Intel"). Next, the Office Action has rejected claims 8 and 17 under 35 U.S.C. §103(a) as being obvious over Lin in view of Intel and further in view of the cited portions of U.S. Patent No. 3,993,891 to Beck et al. (hereinafter "Beck"). Finally, the Office Action has rejected claims 23-24 under 35 U.S.C. §103(a) as being obvious over Lin in view of Intel and further in view of the cited portions of U.S. Patent No. 6,141,675 to Slavenburg et al. (hereinafter "Slavenburg").

Applicants believe required limitations and the motive to make the suggested combinations is lacking along with any likelihood of success in making those combinations. Further, many of the dependent claims are not taught or suggested in Lin, contrary to what is set forth by the Office. Reconsideration is respectfully requested.

Missing Limitation: Multiple Operands Used with Immediate Form

All claims require use of an immediate form with multiple operands. A clear understanding of the immediate form of instruction may assist the Office in understanding the novelty of this limitation. Immediate form instructions specify a value in the Op Code form of

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the instruction. This avoids getting the value from the register file during execution. More specifically:

Claim 1 defines a "plurality of second operands are equal in value to an immediate value."

Claim 9 specifies that "the third and fourth operands are an immediate value specified in an instruction."

Claim 18 requires performing an arithmetic function with the immediate value and the first and second operands.

The Intel reference relates to the '251 series microcontroller. The '251 microcontroller is not a superscalar processor such that any immediate form of instruction would not operate on multiple operands at one time. For example, the Intel cite for this proposition on page 14 (i.e., ADD A,#data) is the pseudo code for adding the immediate value #data to a single register, the accumulator register. There is nothing in this reference that fairly teaches or suggests that an immediate value would affect multiple operands. The Office is respectfully requested to reconsider the rejection.

Motive to Combine Lin and Intel

Applicant only notes in passing that no cite is given for the motivation to combine Lin and Intel. Final Office Action, page 4, first paragraph, last sentence; Advisory Action, page 2, part 11, first paragraph. Because there is no cite in either action, it is unclear to the Applicant where the motivation to combine comes from. The Office is respectfully requested to clarify if Official Notice is the source of this motivation. Should the rejection be maintained and Official Notice is relied upon, an express showing of proof is respectfully requested as set forth in MPEP 2144.03.

Reasonable Likelihood of Success In Combining Lin and Intel

The obviousness test requires a reasonable likelihood of success in making the suggested combination. As understood by the Applicants, the independent claims are combined by using Lin for all elements except use of an immediate value, which relies upon Intel for that

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teaching. Picking and choosing features and inserting them in the suggested manner for such complex systems would have little likelihood of success without undue experimentation. To say differently, trivializes the substantial effort required to design and implement these types of systems.

This problem can be demonstrated by trying to combine these references. Lin provides instruction syntax in Fig. 6, where there are two source registers and a destination register. The ADD instruction cited from Intel, adds an immediate value (#data) to an accumulator register (A). It is not clear how an 8-bit immediate value from Intel could be added to the instruction syntax Lin. The space reserved for the source register addresses (SRC1, SRC2) in Lin are only 5 bits. It is not clear how the instruction syntax would be modified to allow such a combination.

Also, the Intel reference is for a 16-bit processor that doesn't provide for a multiple results to be in a destination register. Any immediate teaching of Intel would have to be expanded to provide for this capability and Lin is no help because of the lack of teaching for an immediate value.

Applicants posit that the combination would have no likelihood of success. Microprocessor designs are the most complex and unpredictable digital designs produced today. For example, Intel is purported to have spent 13 years and multiple-billions developing their Itanium microprocessor. Often several iterations or steppings of the design are required before the microprocessor works properly. To take the position that components from various designs can be interchanged so easily simply goes too far. Reconsideration is respectfully requested.

Teachings Missing from the Cited References for Dependent Claims

The dependent claims, some amended, provide limitations neither taught nor suggested by the cited references. More specifically, claims 4-6, 12, 13, and 15 require further explanation as to why Lin teaches these limitations. The Advisory Action appears to say that Lin teaches these limitations. As noted in every response by the Applicant, Lin does not teach or

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suggest use of immediate values. Any reliance upon Lin is not reasonably supported by that reference.

Claim 5 requires the immediate value be signed. The Office takes the position that Lin teaches this limitation. Final Office Action, page 4, second-to-last paragraph; Advisory Action, page 2, last paragraph. Earlier, the final Office Action takes the position that Lin doesn't teach an immediate value. It is not clear how Lin could teach signing the immediate value when it doesn't even teach use of any immediate forms of instructions.

In claim 6, there is a limitation to scaling the immediate value. The Office sets forth the saturation ability of Lin for this proposition. Final Office Action, page 4, last paragraph; Advisory Action, page 2, last paragraph; Advisory Action, page 2, last paragraph. Those skilled in the art appreciate that saturation has nothing to do with prescaling.

Claims 4, 12 and 13 require a number of bits for the immediate value. The carry-in bit is cited by the Office as the positive integer. The claims are refined to require multiple bits.

In claim 15, the scaling factor is required to be divisible by two. Lin doesn't teach or suggest scaling as set forth above in relation to claim 6. The Office takes the position that saturation is scaling in the final Office Action, which is simply not true. Final Office Action, page 6, last paragraph. In reviewing the Advisory Action, it is not clear to the Applicant what the Office is arguing. Advisory Action, page 2, last sentence.

To cite Lin, which doesn't teach or suggest use of an immediate value, for limitations that require use of an immediate form instruction is believed the Applicants to be unreasonable. Reconsideration of these rejections is respectfully requested.

CONCLUSION

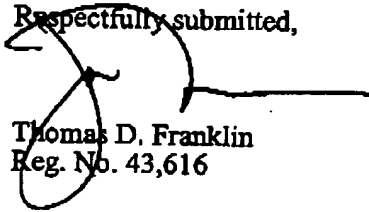
In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

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If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,


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